DIGITAL PATTERN GENERATING CIRCUIT

Patent number: JP57185720
Publication date: 1982-11-16
Inventor: TAKETOMI TOSHIKATSU
Applicant: AKAI DENKI KK
Classification:
- international: H03K3/78
- european:
Application number: JP19810071190 19810511
Priority number(s):

Abstract of **JP57185720**

PURPOSE:To simplify the pattern change, by using a counter output as an address for read only memory (ROM) and storing a desired digital pattern in the ROM.
CONSTITUTION:A counter 1 counts a clock pulse CP and an output of each digit of the counter is given to an ROM2 as an address. A storage content to output a desired digital pattern is stored in the ROM2 and a desired digital pattern is obtained at terminals 01 and 02.